Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **N. CLR1**
2. **D1**
3. **CLK1**
4. **N. PRE1**
5. **Q1**
6. **N. Q1**
7. **GND**
8. **N. Q2**
9. **Q2**
10. **N. PRE2**
11. **CLK2**
12. **D2**
13. **N. CLR2**
14. **VCC**

**.041”**

**3 4 5**

**11 10**

**12**

**13**

**14**

**1**

**2**

**+**

**9**

**8**

**7**

**6**

**.061”**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: GND**

**APPROVED BY: DK DIE SIZE : .041 X .061” DATE: 9/22/21**

**MFG: SIGNETICS THICKNESS: .015” P/N: 54S74**

**DG 10.1.2**

#### Rev B, 7/19/02